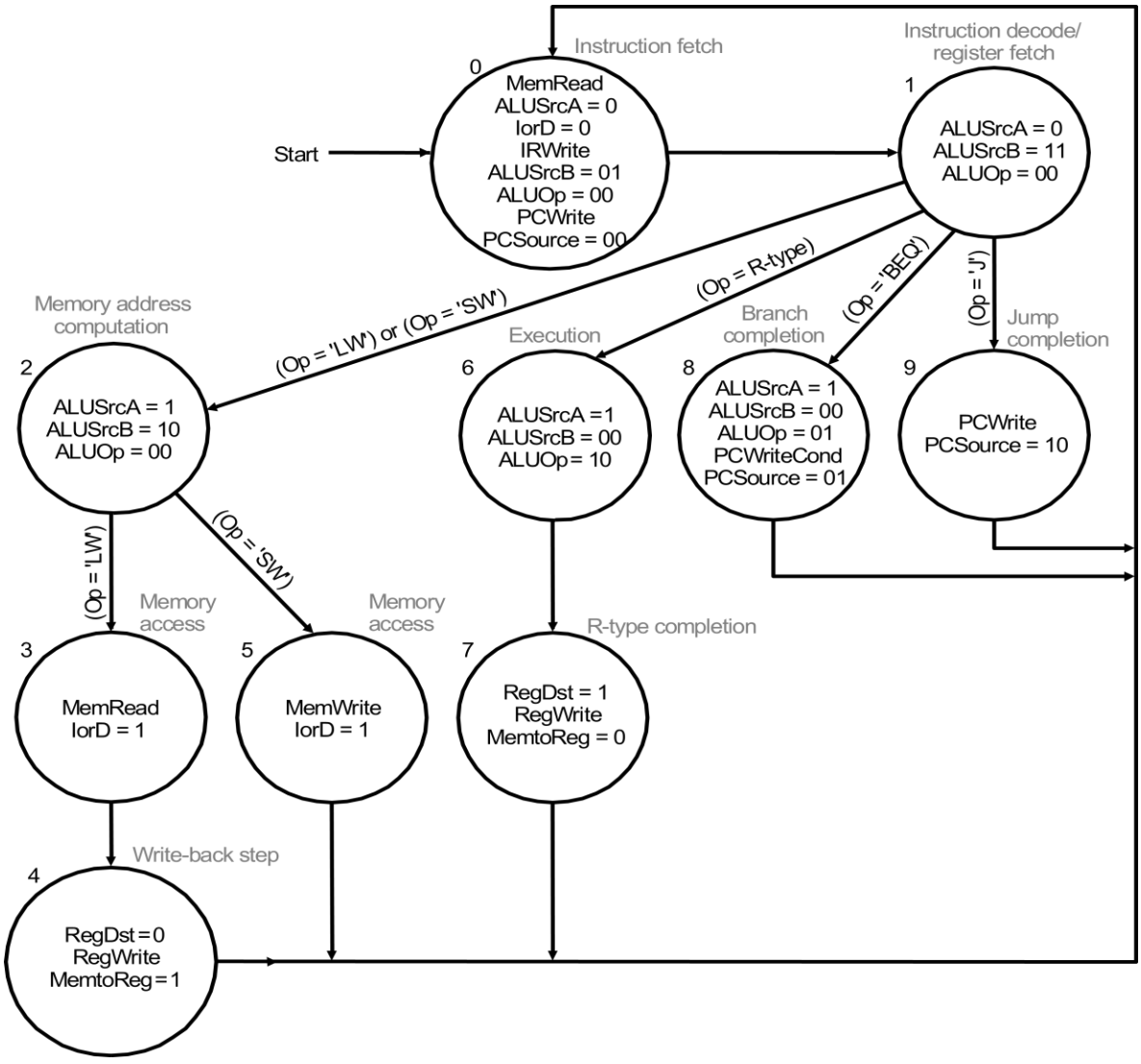
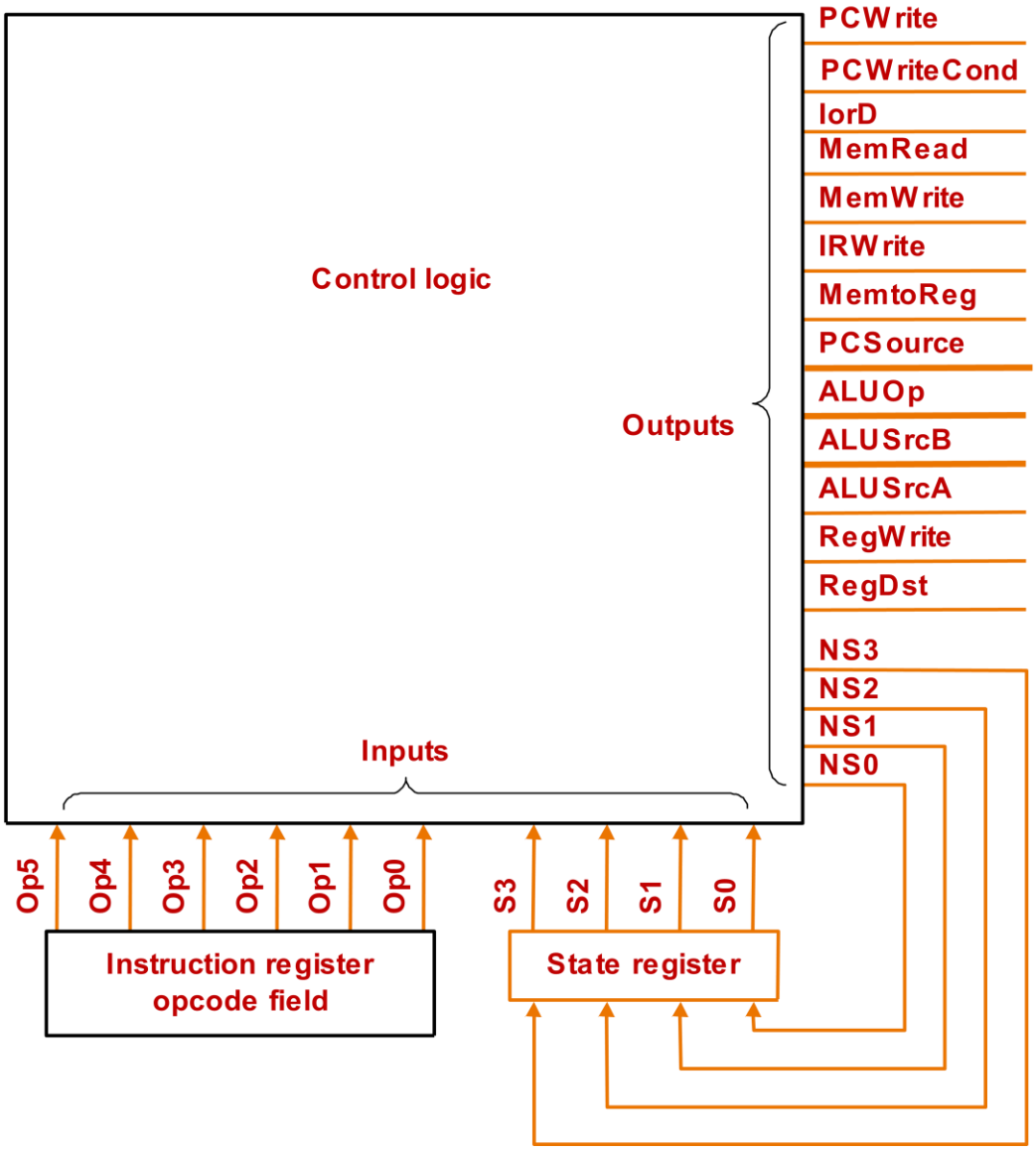
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
CS C342 Computer Architecture
Lab Sheet - 7

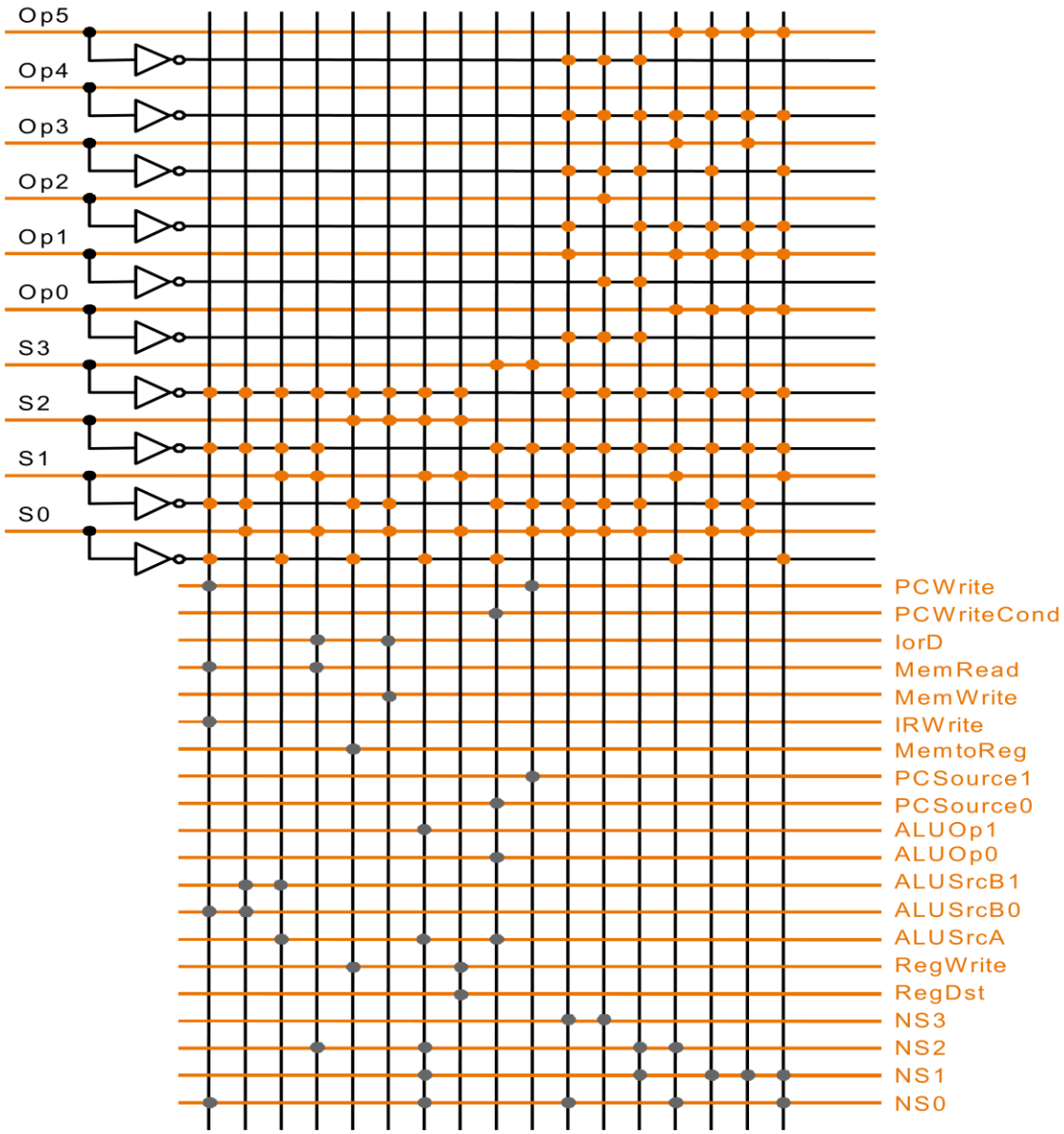
In this lab you will design the Main controller for MIPS multicycle implementation. The controller has 10 states as shown below.



The controller has 16 outputs + 4 next state signals. It has a total of 10 inputs (6 opcode bits + 4 present state bits). The block diagram of controller is shown below.



The equations governing the input/output relations for the controller can be derived from the figure given below, which shows its PLA implementation.



Upper half is the AND plane that computes all the products. The products are carried to the lower OR plane by the vertical lines. The sum terms for each output is given by the corresponding horizontal line E.g., IorD = S0.S1.S2'.S3' + S0.S1'.S2.S3'

Write the Verilog code for the controller. Also write a test bench to check the controller for LW instruction.